

What is claimed is:

1 1. A read-only memory cell, comprising:
2 a substrate;
3 a plurality of bit lines, formed near the surface of
4 the substrate;
5 a plurality of bit line oxides, disposed over the
6 bit lines;
7 a gate dielectric layer, disposed over the substrate
8 between the bit lines, the gate dielectric
9 layer comprising a silicon-rich oxide layer;
10 and
11 a word line, disposed over the bit line oxides and
12 the gate dielectric layer.

1 2. The cell as claimed in claim 1, wherein the
2 gate dielectric layer further comprises a first gate
3 oxide layer, disposed between the silicon-rich oxide
4 layer and the substrate.

1 3. The cell as claimed in claim 1, wherein the
2 gate dielectric layer further comprises a second gate
3 oxide layer, disposed between the silicon-rich oxide
4 layer and the bit lines.

1 4. The cell as claimed in claim 1, wherein the
2 silicon-rich oxide layer is further disposed between the
3 word line and the bit line oxides.

1 5. A method for fabricating a read-only memory
2 cell, comprising the steps of:
3 providing a substrate;

4 forming a first gate oxide layer on the substrate;
5 defining a bit line pattern in the first gate oxide
6 layer and forming a plurality of bit line
7 openings;
8 forming a plurality of doping areas in the substrate
9 near its surface in the bit line openings as
10 bit lines;
11 forming a plurality of bit line oxides in the bit
12 lines;
13 forming a silicon-rich oxide layer over the first
14 gate oxide layer;
15 forming a second gate oxide layer on the silicon-
16 rich oxide layer; and
17 forming a conductive layer over the second gate
18 oxide layer and the bit line oxides.

1 6. The method as claimed in claim 5, wherein the
2 first gate oxide layer is formed by thermal oxidation.

1 7. The method as claimed in claim 5, wherein the
2 first gate oxide layer is formed by chemical vapor
3 deposition.

1 8. The method as claimed in claim 5, wherein the
2 doping area is formed by phosphorus ion implantation.

1 9. The method as claimed in claim 5, wherein the
2 silicon-rich oxide layer is formed by plasma chemical
3 vapor deposition.

1 10. The method as claimed in claim 9, wherein the
2 plasma chemical vapor deposition uses Tetraethylor-
3 thosilicate (TOES) as precursor.

1 11. The method as claimed in claim 9, wherein the
2 plasma chemical vapor deposition uses SiH_4 as precursor.

1 12. The method as claimed in claim 5, wherein the
2 second gate oxide layer is formed by chemical vapor
3 deposition.